Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1-3. (Cancelled).

4. (Previously Presented) The display of claim 17, wherein in order to install said control circuit in a control circuit accommodation portion of said TFT substrate, said control circuit accommodation portion is made thinner than other portions of said TFT substrate.

5. (Cancelled).

6. (Previously Presented) The display of claim 17, wherein said control circuit is packed over said TFT substrate by COG (chip-on-glass) technology.

7-12. (Cancelled).

13. (Previously Presented) The method of claim 24, further comprising the step of thinning a portion of said counter substrate which is located opposite to a control circuit for controlling said driver circuit made up of said driver TFTs, to install said control circuit.

14. (Previously Presented) The method of claim 24, wherein said control circuit is packed over said TFT substrate by COG (chip-on-glass) technology.

15-16. (Cancelled).

17. (Previously Presented) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a TFT substrate and arrayed in a matrix;

a counter substrate located opposite to said TFT substrate;

a layer of a liquid crystal material provided between said TFT substrate and said counter substrate;

a sealing material sealing around said liquid crystal material and provided between said TFT substrate and said counter substrate;

a driver TFT provided over said TFT substrate; and

a control circuit comprising a control circuit chip sealed in said sealing material, said control circuit provided over TFT substrate for controlling said driver TFT.

18-20. (Cancelled).

21. (Previously Presented) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a TFT substrate and arrayed in a matrix;

a bus line provided over said TFT substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said TFT substrate;

a layer of a liquid crystal material provided between said TFT substrate and said counter substrate;

a sealing material sealing around said liquid crystal material and provided between said TFT substrate and said counter substrate;

a driver TFT provided over said TFT substrate; and

a control circuit comprising a control circuit chip sealed in said sealing material, said control circuit provided over said TFT substrate for controlling said driver TFT.

22. (Previously Presented) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a TFT substrate and arrayed in a matrix;

a counter substrate located opposite to said TFT substrate;

a layer of a liquid crystal material provided between said TFT substrate and said counter substrate;

a sealing material sealing around said liquid crystal material and provided between said TFT substrate and said counter substrate, said sealing material being provided outside at least said pixel TFTs;

a driver TFT provided over said TFT substrate; and

a control circuit comprising a control circuit chip sealed in said sealing material, said control circuit provided over said TFT substrate for controlling said driver TFT.

23. (Previously Presented) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a TFT substrate and arrayed in a matrix;

a bus line provided over said TFT substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said TFT substrate;

a layer of a liquid crystal material provided between said TFT substrate and said counter substrate;

a sealing material sealing around said liquid crystal material and provided between said TFT substrate and said counter substrate, said sealing material being provided outside at least said pixel TFTs;

a driver TFT provided over said TFT substrate; and

a control circuit comprising a control circuit chip sealed in said sealing material, said control circuit provided over said TFT substrate for controlling said driver TFT.

24. (Previously Presented) A method of fabricating an active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a TFT substrate and arrayed in a matrix;

a bus line provided over said TFT substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said TFT substrate;

a layer of a liquid crystal material provided between said TFT substrate and said counter substrate;

a sealing material sealing around said liquid crystal material and provided between said TFT substrate and said counter substrate and outside at least said pixel TFTs;

a driver TFT provided over said TFT substrate; and

a control circuit comprising a control circuit chip sealed in said sealing material, said control circuit provided over said TFT substrate for controlling said driver TFT,

said method comprising:

cutting said TFT substrate and said counter substrate outside said sealing material having said control circuit sealed in said sealing material.

25. (Previously Presented) A method of fabricating an active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a TFT substrate and arrayed in a matrix;

a bus line provided over said TFT substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said TFT substrate;

a layer of a liquid crystal material provided between said TFT substrate and said counter substrate;

a sealing material sealing around said liquid crystal material and provided between said TFT substrate and said counter substrate;

a driver TFT provided over said TFT substrate; and

a control circuit comprising a control circuit chip sealed in said sealing material, said control circuit provided over said TFT substrate for controlling said driver TFT,

said method comprising:

cutting said TFT substrate and said counter substrate outside said sealing material having said control circuit sealed in said sealing material.

26-29. (Cancelled).

30. (Previously Presented) The display of claim 21, wherein in order to install said control circuit in a control circuit accommodation portion of said TFT substrate, said counter substrate has a thinned portion located opposite to said control circuit accommodation portion.

31. (Previously Presented) The display of claim 21, wherein said control circuit is packed over said TFT substrate by COG (chip-on-glass) technology.

32-34. (Cancelled).

35. (Previously Presented) The display of claim 22, wherein in order to install said control circuit in a control circuit accommodation portion of said TFT substrate, said counter substrate has a thinned portion located opposite to said control circuit accommodation portion.

36. (Previously Presented) The display of claim 22, wherein said control circuit is packed over said TFT substrate by COG (chip-on-glass) technology.

37-39. (Cancelled).

40. (Previously Presented) The display of claim 23, wherein in order to install said control circuit in a control circuit accommodation portion of said TFT substrate, said counter substrate has a thinned portion located opposite to said control circuit accommodation portion.

41. (Previously Presented) The display of claim 23, wherein said control circuit is packed over said TFT substrate by COG (chip-on-glass) technology.

42. (Cancelled).

43. (Cancelled).

44. (Previously Presented) The method of claim 25, further comprising the step of thinning a portion of said counter substrate which is located opposite to said control circuit, to install said control circuit.

45-60. (Cancelled).

61. (Currently Amended) A semiconductor device including ~~at least~~ one liquid crystal panel comprising a TFT substrate and a counter substrate,

wherein said TFT substrate and said counter substrate each comprises ~~having at least~~ a first side edge, a second side edge, a third side edge, and a fourth side edge;~~, said liquid crystal panel comprising:~~

wherein said ~~a~~ TFT substrate ~~comprising~~ comprises a glass; and

wherein said counter substrate is located opposite to said TFT substrate,

said semiconductor device comprising:

a pixel TFT provided over said TFT substrate;

a channel formation region provided in a semiconductor film provided over said TFT

substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

~~a counter substrate located opposite to said TFT substrate;~~

a bus line provided over said TFT substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said TFT substrate;

a sealing material provided between said TFT substrate and said counter substrate; and

a nonconductive material applied to the first side edge, the second side edge, and the third side edge of said TFT substrate and said counter substrate of said liquid crystal panel,

wherein said nonconductive material is provided on an outer side of said sealing material, and

wherein said nonconductive material is not applied to the fourth side edge of said TFT substrate and said counter substrate of said liquid crystal panel.

62. (Currently Amended) A semiconductor device including ~~at least~~ one liquid crystal panel comprising a TFT substrate and a counter substrate,

wherein said TFT substrate and said counter substrate each comprises ~~having at least~~ a first side edge, a second side edge, a third side edge, and a fourth side edge;~~, said liquid crystal panel comprising:~~

wherein said ~~a~~ TFT substrate ~~comprising~~ comprises a glass; and

wherein said counter substrate is located opposite to said TFT substrate,

said semiconductor device comprising:

a pixel TFT provided over said TFT substrate;

a channel formation region provided in a semiconductor film provided over said TFT substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

~~a counter substrate located opposite to said TFT substrate;~~

a bus line provided over said TFT substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said TFT substrate;

a sealing material provided between said TFT substrate and said counter substrate; and

a weakly conductive material applied to the first side edge, the second side edge, and the third side edge of said TFT substrate and said counter substrate of said liquid crystal panel,

wherein said weakly conductive material is provided on an outer side of said sealing material, and

wherein said weakly conductive material is not applied to the fourth side edge of said TFT substrate and said counter substrate of said liquid crystal panel.

63. (Currently Amended) A semiconductor device including ~~at least~~ one liquid crystal panel comprising a TFT substrate and a counter substrate,

wherein said TFT substrate and said counter substrate each comprises ~~having at least~~ a first side edge, a second side edge, a third side edge, and a fourth side edge;~~, said liquid crystal panel comprising:~~

wherein said ~~a~~ TFT substrate ~~comprising~~ comprises a glass; and

wherein said counter substrate is located opposite to said TFT substrate,

said semiconductor device comprising:

a pixel TFT provided over a TFT substrate;

a channel formation region provided in a semiconductor film provided over said TFT substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

a driver TFT provided over said TFT substrate;

~~a counter substrate located opposite to said TFT substrate;~~

a bus line provided over said TFT substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said TFT substrate;

a sealing material provided between said TFT substrate and said counter substrate; and

a nonconductive material applied to the first side edge, the second side edge, and the third side edge of said TFT substrate and said counter substrate of said liquid crystal panel,

wherein said nonconductive material is provided on an outer side of said sealing material, and

wherein said nonconductive material is not applied to the fourth side edge of said TFT substrate and said counter substrate of said liquid crystal panel.

64. (Currently Amended) A semiconductor device including ~~at least~~ one liquid crystal panel comprising a TFT substrate and a counter substrate,

wherein said TFT substrate and said counter substrate each comprises ~~having at least~~ a first side edge, a second side edge, a third side edge, and a fourth side edge;~~, said liquid crystal panel comprising:~~

wherein said ~~a~~ TFT substrate ~~comprising~~ comprises a glass; and

wherein said counter substrate located opposite to said TFT substrate,

said semiconductor device comprising:

a pixel TFT provided over a TFT substrate;

a channel formation region provided in a semiconductor film provided over said TFT substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

a driver TFT provided over said TFT substrate;

~~a counter substrate located opposite to said TFT substrate;~~

a bus line provided over said TFT substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said TFT substrate;

a sealing material provided between said TFT substrate and said counter substrate; and

a weakly conductive material applied to the first side edge, the second side edge, and the third side edge of said TFT substrate and said counter substrate of said liquid crystal panel,

wherein said weakly conductive material is provided on an outer side of said sealing material, and

wherein said weakly conductive material is not applied to the fourth side edge of said TFT substrate and said counter substrate of said liquid crystal panel.

65-72. (Cancelled).